Detector Support Group

We choose to do these things "not because they are easy, but because they are hard".

Weekly Report, 2021-06-23

Summary

Hall A – GEM

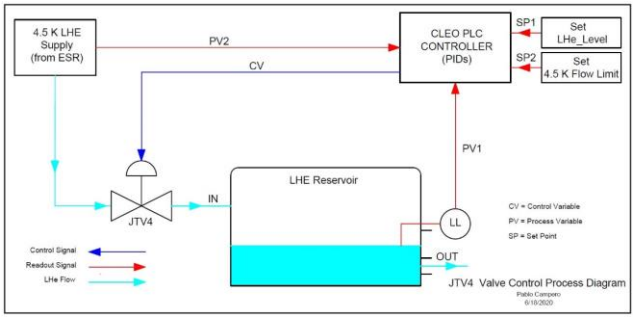
Mary Ann Antonioli, Peter Bonneau, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Tested six SBS GEM gas flow chassis

Hall A – SoLID

Mary Ann Antonioli, Pablo Campero, Mindy Leffel, Marc McMullen

- Completed, and generated PDFs for, electrical drawings: *Electric Linear Actuator Drive Motors, Valve Motor Drivers Wire Diagram*
- Updated *Cable List* spreadsheet
- Generated flowchart and process diagram showing PID controls for *JTV4 He Top Fill* valve

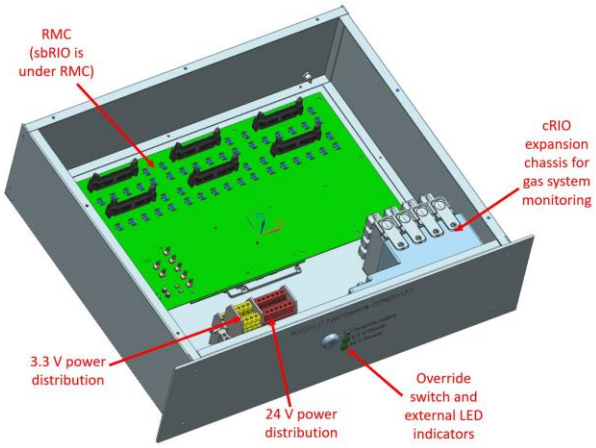


Process diagram showing PID controls for *JTV4 He Top Fill* valve

Hall B – RICH-II

Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Tyler Lemon

- Assembled manual alignment stand for new reflectivity test station
- Modified design of hardware interlock chassis using NX12



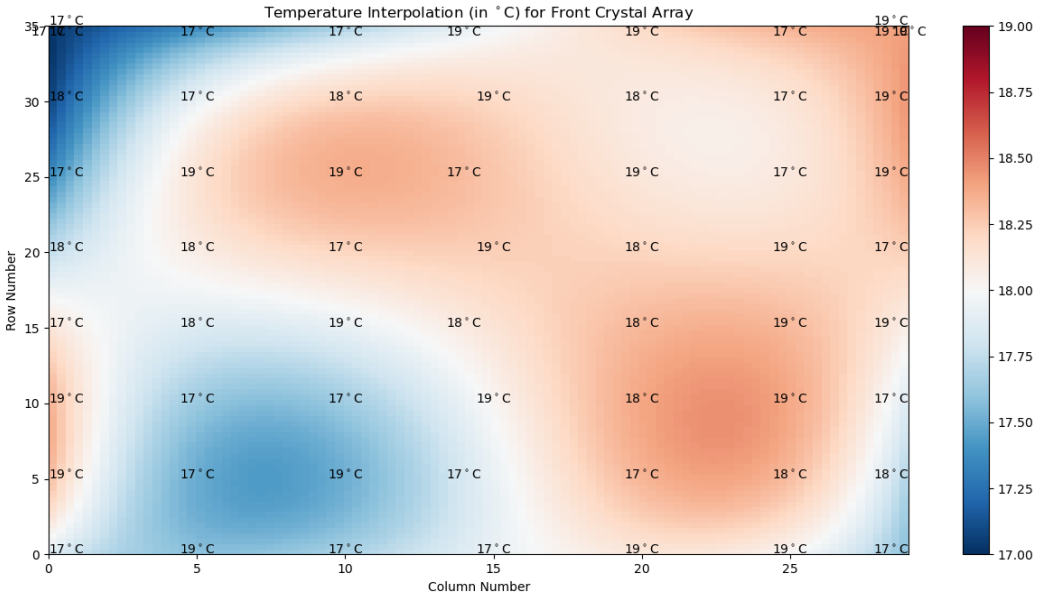
3U tall and 15" deep interlock chassis in NX12.

- Completed first version of LabVIEW front panel for the Hardware Interlock System
- Completed detailed cost estimate for air cooling and N_2 purge systems
- Developing routing of the RMC PCB
- Developing schematic for the backplane PCB

Hall C – NPS

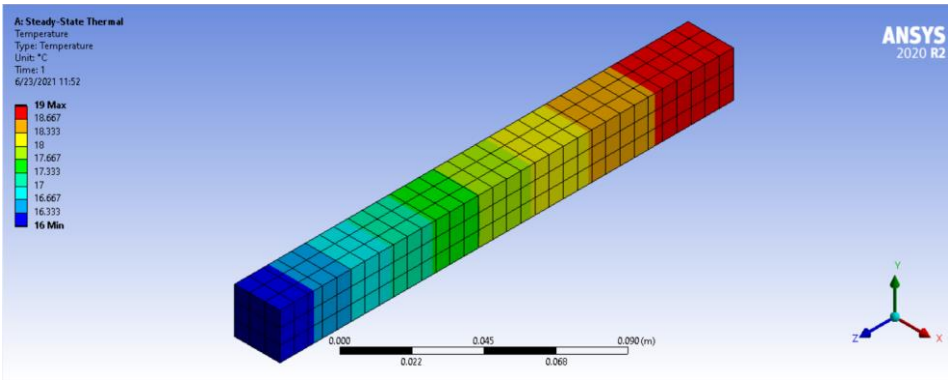
Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen

- Modified surface plot of front crystal zone temperatures generated using random values
  - ✶ Researching interpolation methods to improve plot



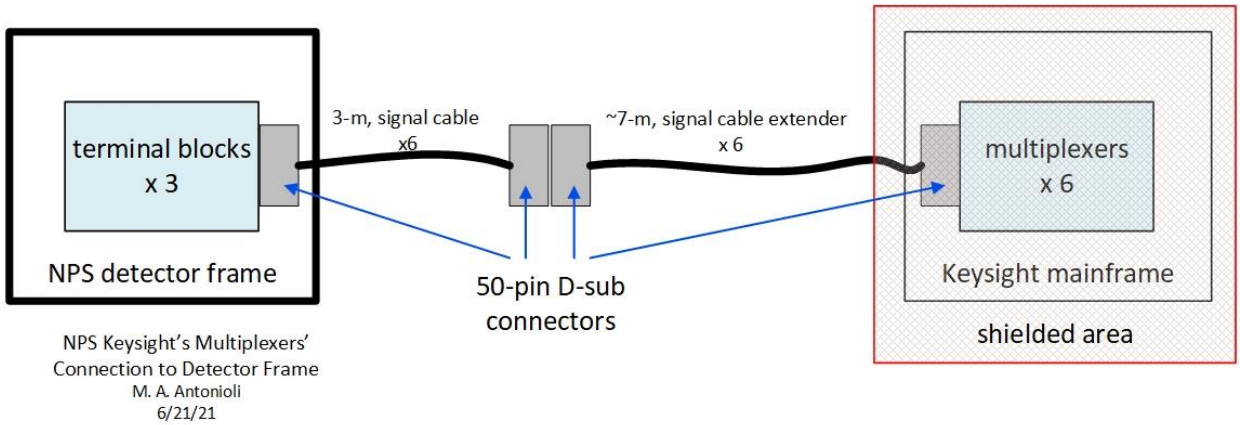
Surface plot of front crystal zone temperatures with randomly generated values displayed

- Developing thermal analysis of crystal zone using ANSYS
  - ✶ Generated thermal simulation for single $PbWO_4$ crystal; boundary conditions were 16°C and 19°C (front and back, respectively)



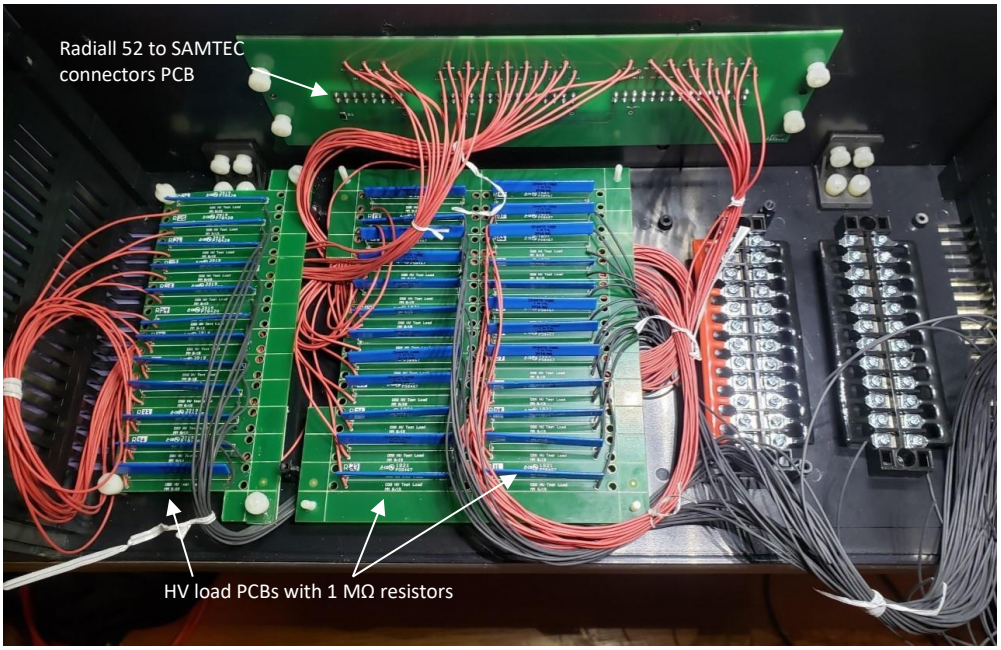
Thermal simulation of $PbWO_4$ crystal

- Developing LabVIEW front panel for Hardware Interlock System program
  - ✶ Completed code for averaging and displaying crystal zone cooling circuit temperatures
- Generated Visio drawing of connections from terminal blocks located in detector frame to Keysight mainframe to be located in shielded area



Drawing showing the connection between the terminal blocks in the detector frame and the Keysight mainframe

- Trimmed Radiall 52 connector screws and heated heat shrink for the last eight of the 40 HV supply cables
- Long-term load testing of HV supply cables: 30 of 40 cables complete
- Populated four PCBs for the new HV supply cable test chassis – one Radiall 52 to SAMTEC test board and three HV test load boards



Interior of new HV supply cable test chassis showing three PCBs populated with 1 MΩ resistors

EIC

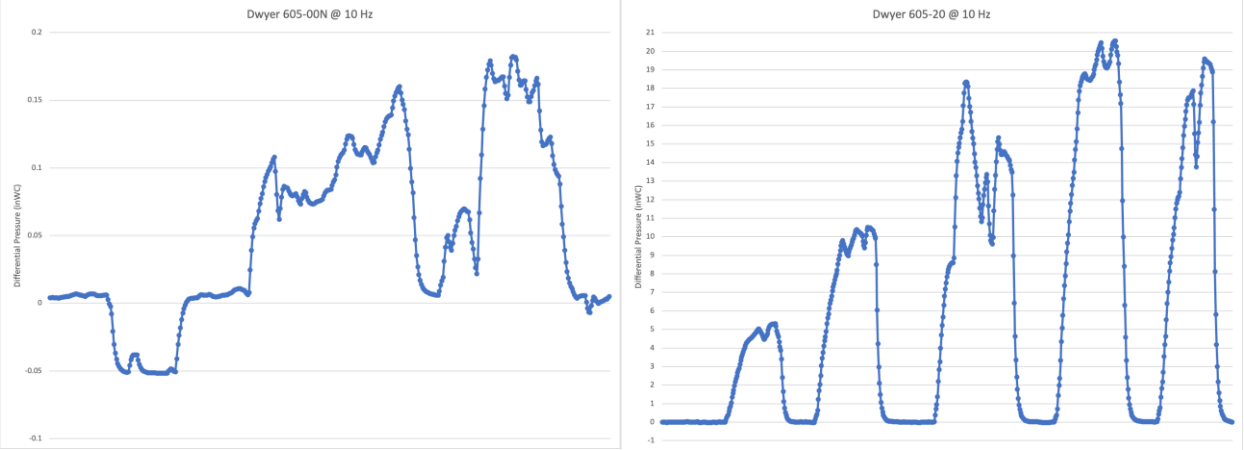
Brian Eng

- Attended ECCE and ATHENA tracking detectors meetings (two of the collaborations forming for EIC)
- Generating summary table for various readouts for the tracking detectors

DSG R&D - GEM

Brian Eng

- Testing Raspberry Pi ADC board with Dwyer differential pressure indicators with built-in transmitters (models 605-00N and 605-20)
    - ✶ Both transmitters read a bit lower than the dial, but this is probably due to improper mounting and unevenly applied pressure (at home test set up)



Plots of differential pressure (inWC) generated during testing of Dwyer 605-00N (left) and 605-20 (right) differential pressure indicators